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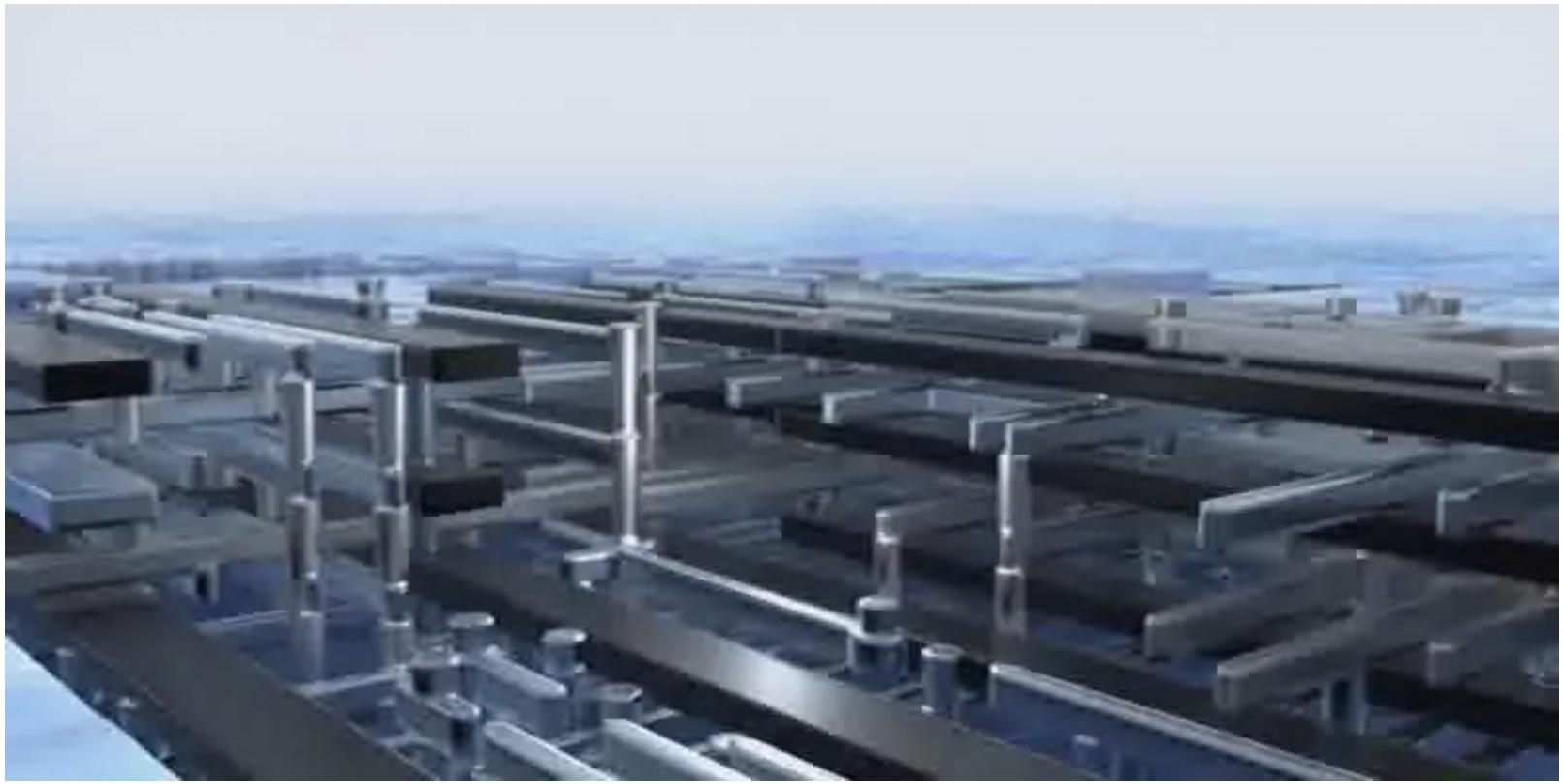
Lithographic Challenges

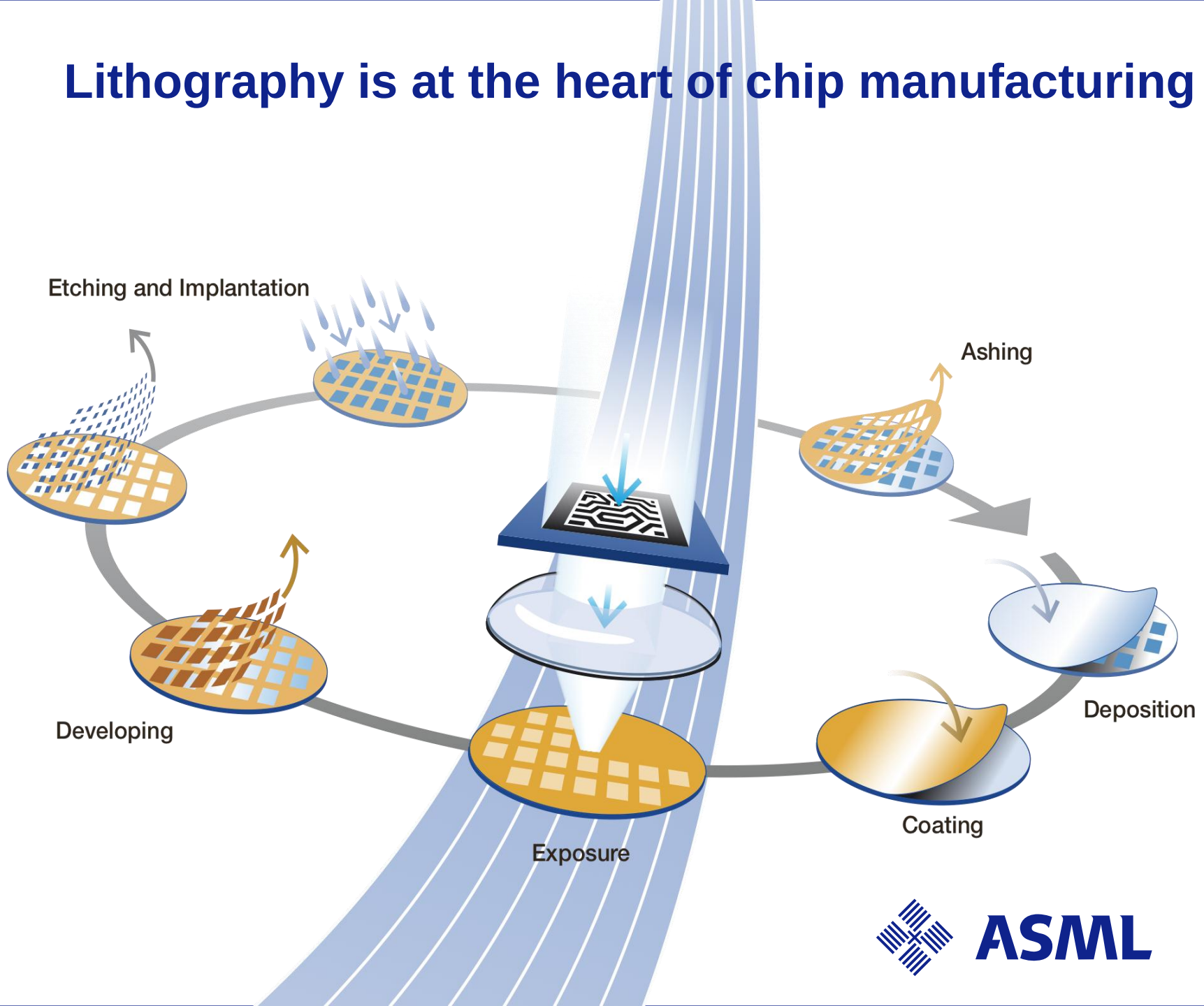
an ASML perspective

Boudewijn Sluijk, Intel ERIC, Dublin, 4 Oct. 2012

Zoom into a wafer: this is nanometer accuracy



Lithography is at the heart of chip manufacturing



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Photolithography – how an ASML system works

A line-up of systems in support of Moore's law

In 30 years: From 1,200 nm to less than 20 nm resolution

From <0.5M€ per system to >65M€

R&D: 50 M€

1984:

PAS 2000

Resolution: >1μm

overlay: 250 nm

1989:

PAS 5000

Resolution: <500 nm

overlay: 100 nm

R&D: 400 M€

1990's:

PAS 5500 steppers/scanners

Resolution: 400 to 90 nm

overlay: 100 to 12 nm

2000's:

Twinscan

Resolution: 100 to 38 nm

overlay: 20 to 4 nm

NXT:1960Bi

R&D: 1,500 M€ excluding machines

2010's:

NXE EUV systems

Resolution: 32 to <20 nm

overlay: 2 nm

NXE:3300B

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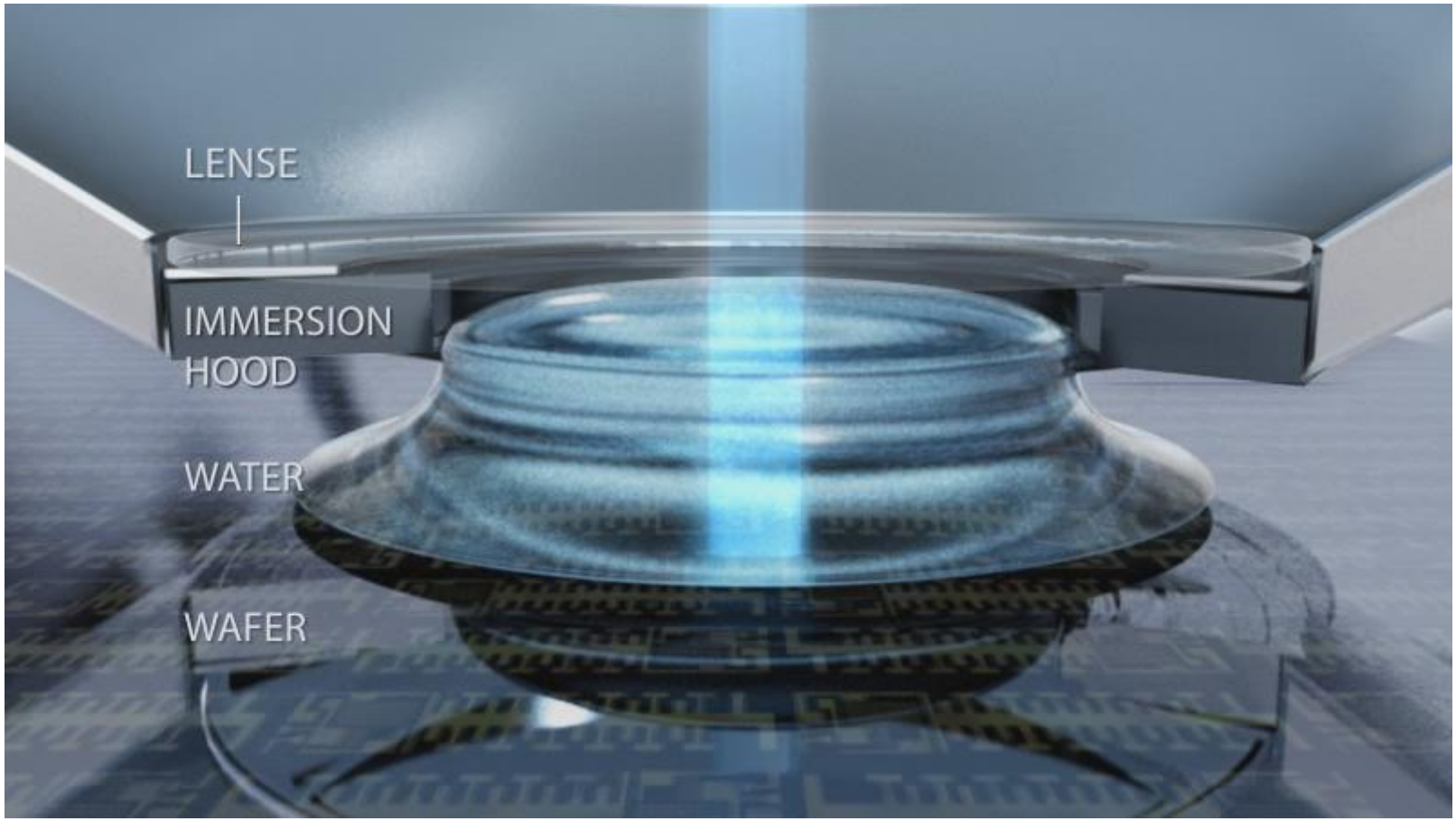
How NXT:1960Bi immersion works:



ArF immersion for cost-efficient Double Patterning and Quadruple Patterning

NXT platform will be ready for all critical layers

Litho Requirements	2010 – 2012 N28	2012 – 2013 N20	2014 – 2015 N14	2015 – 2016 N11
On Product Overlay	9 nm	6 nm	4 nm	3 nm
CD Uniformity iso	3 nm	1.5 nm	1 nm	<1 nm
Total Focus Budget	100 nm	80 nm	60 nm	40 nm

	NXT:1950i + PEP	NXT:1960Bi	NXT-C	Focus / Overlay extension
Timing	Q1'12	Q3'12	Q3'13	H2 '15
DCO/MMO	2.5 / 5.5nm	2.5 / 4.5nm	1.8 / 3.5nm	1.2 / 2.0nm
Full Wafer Focus Unif	30nm	25nm	20nm	15nm
Full Wafer CDU (iso)	3.0nm	2.0nm	1.5nm	1.0nm
Throughput (96 shots)	230 WpH	230 WpH	250 WpH	>250 WpH
Target Availability	→ 95%** (Q2'12)	95%**	97%**	97%*
Defects/Wafer	10	10	<7	<7

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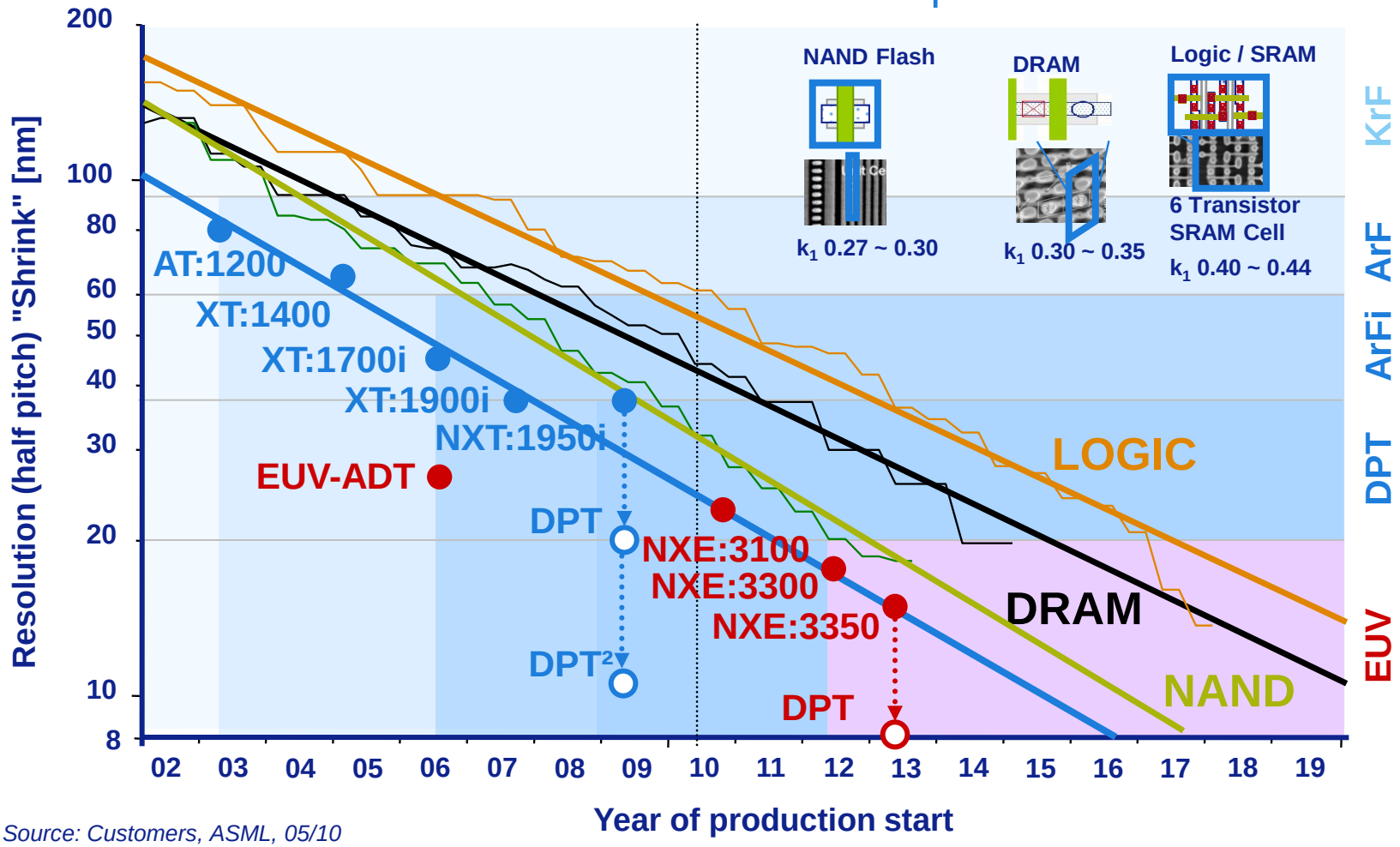
Chip shrink will continue

And ASML will match customers' shrink roadmaps

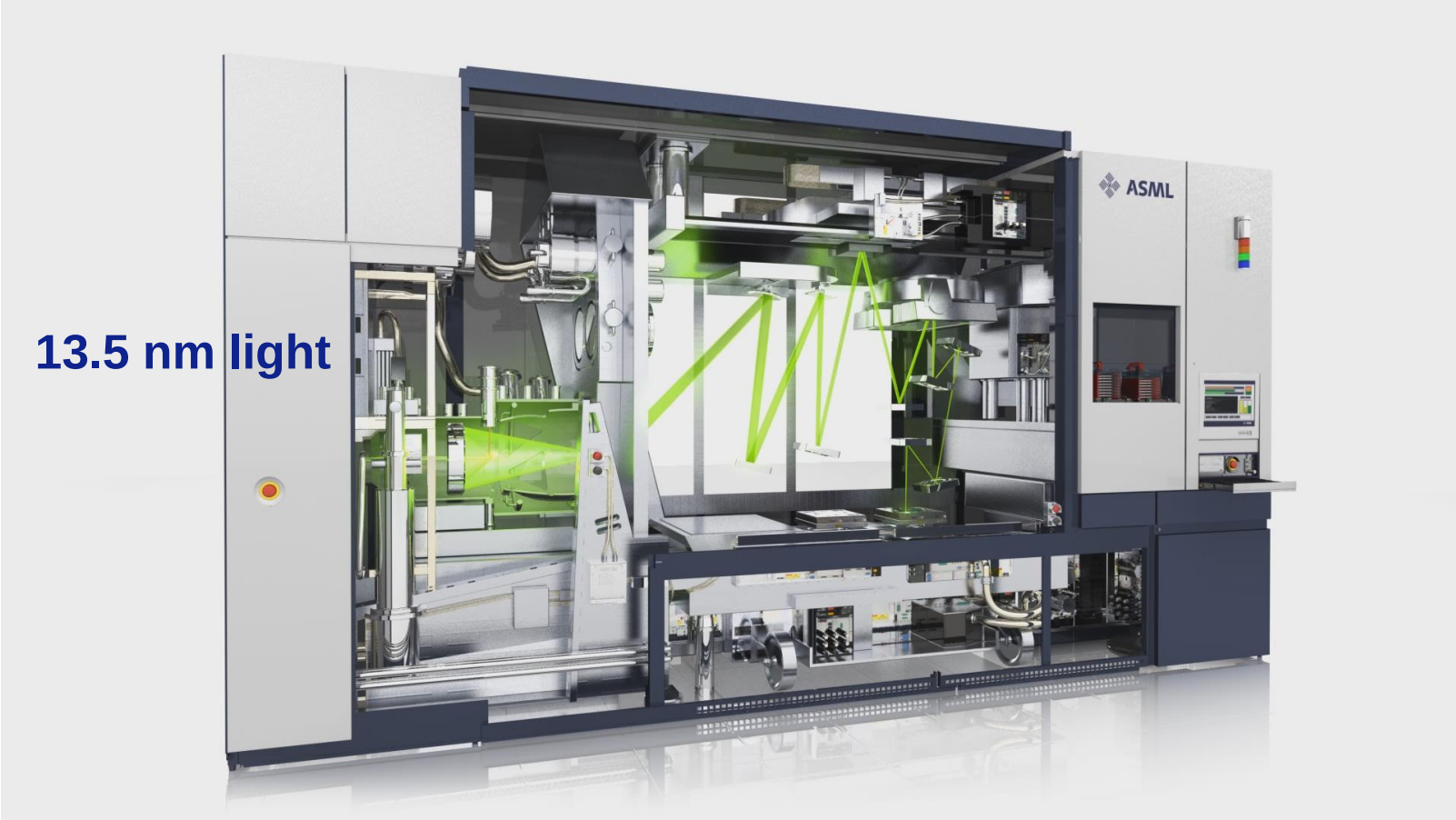


Source: Customers, ASML, 05/10

Notes:
1. R&D solution required 1.5~ 2 yrs ahead of Production
2. EUV resolution requires 7nm diffusion length resist
3. DPT = Double Patterning

Public

EUV: a new light source on mirrors in a vacuum



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The future is here: EUV has arrived in fabs worldwide

System 1
Exposing wafers for device development

System 2
Exposing wafers for device development

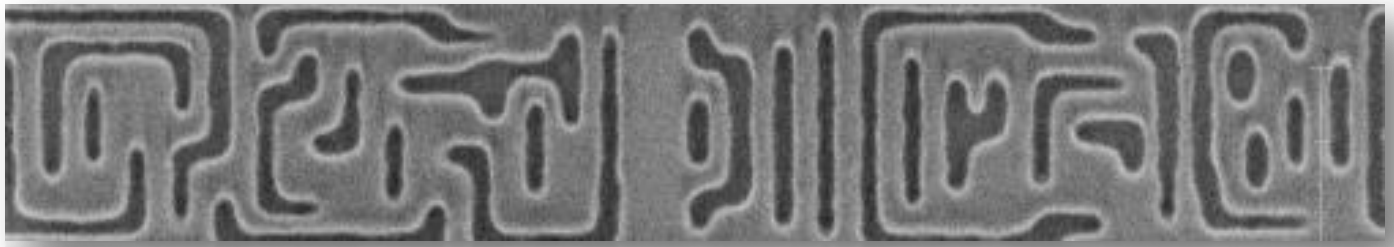
System 3:
Exposing wafers for device development

System 4:
Exposing wafers for device development

System 5:
Exposing wafers for device development

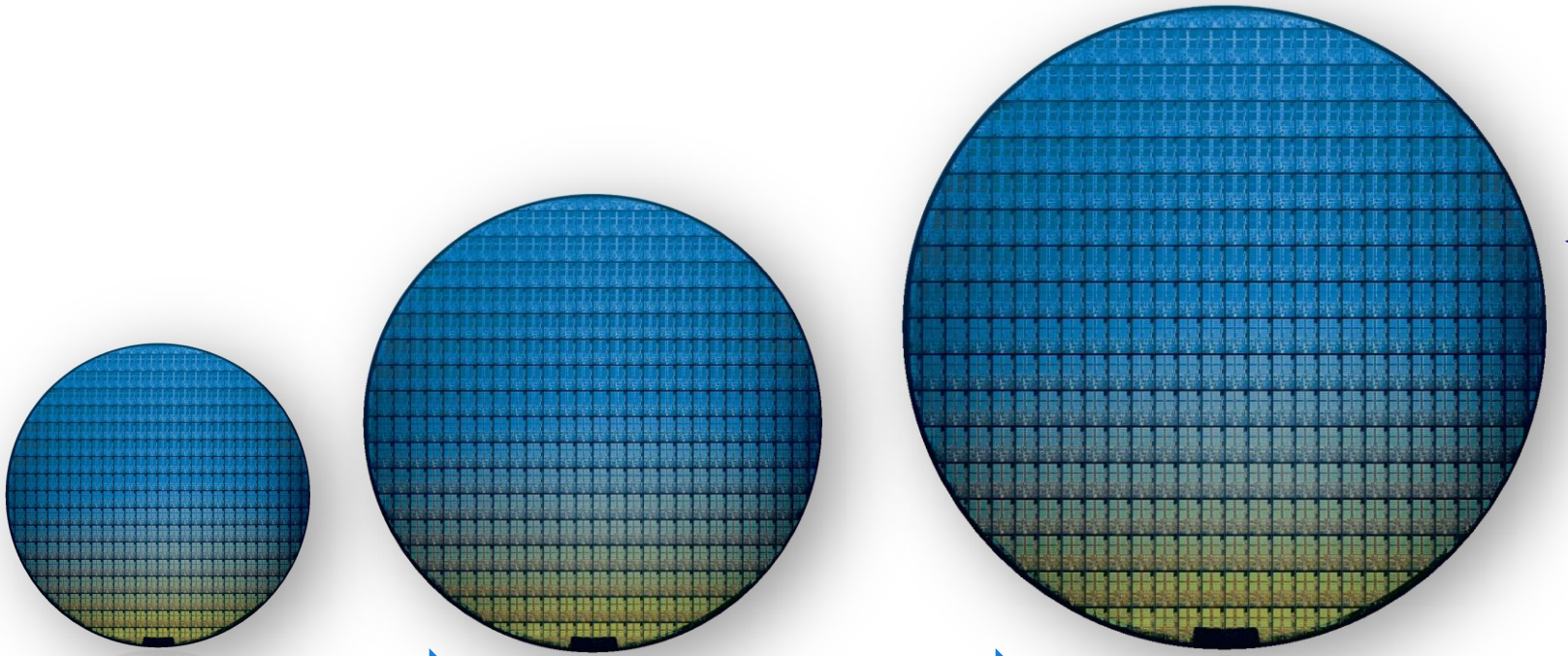
System 6:
Exposing wafers for device development

Single exposure 14nm node metal 1 features



Good printing performance through a focus range of ~100nm for 14nm node ARM M1 clip (46nm min. pitch)

The promise of larger wafers



	200 mm → 300 mm	300 mm → 450 mm
Wafer Area	2.25X	2.25X
Effective Area	2.36X	2.40X
Cost Reduction Goal	30%	30%

Source: Shang-yi, Chiang, TSMC, SPIE march 2011

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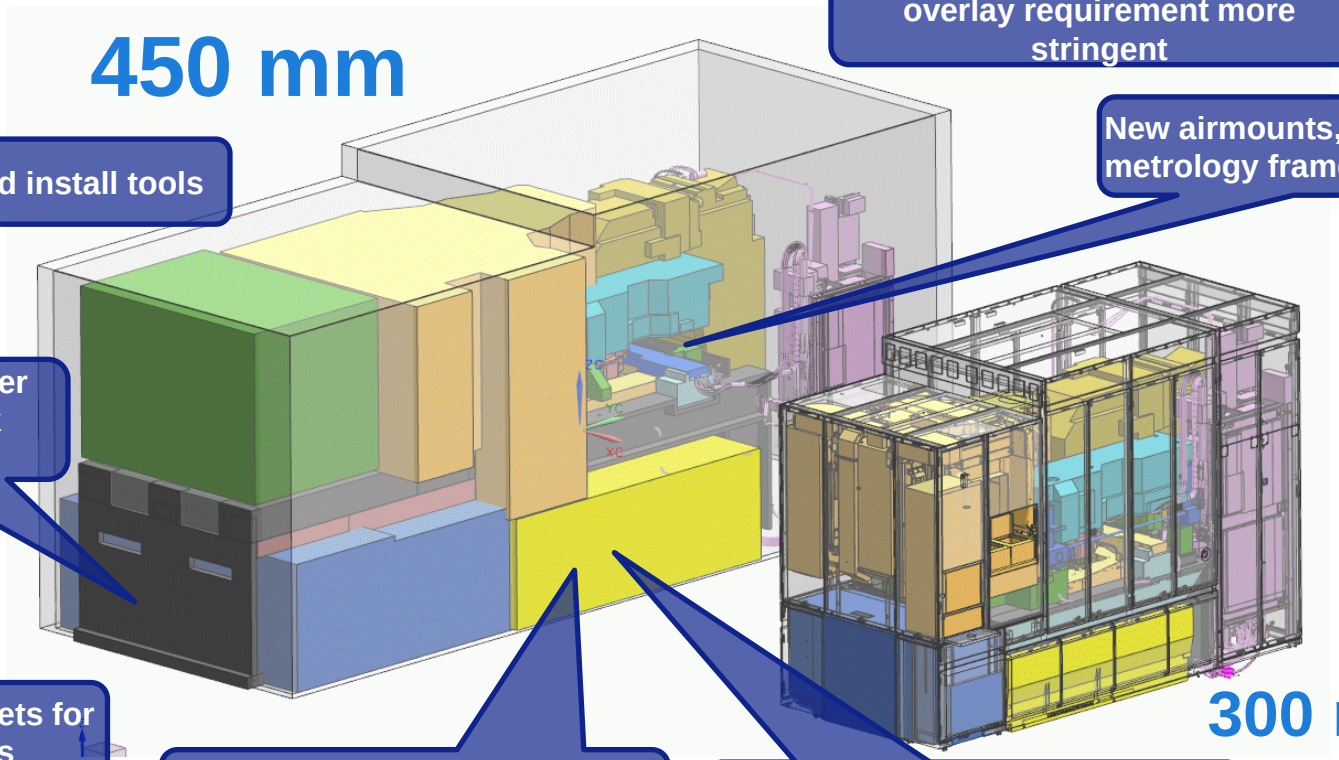
450 mm poses significant engineering challenges



Expose time is double, and overlay requirement more stringent

New airmounts, base frame, metrology frame

New transport and install tools

New 450 mm wafer handler & track interface

New power cabinets for larger stages

450 mm wafer stage, wafer table & grid plates

450 mm SW architecture & metrology adaptions

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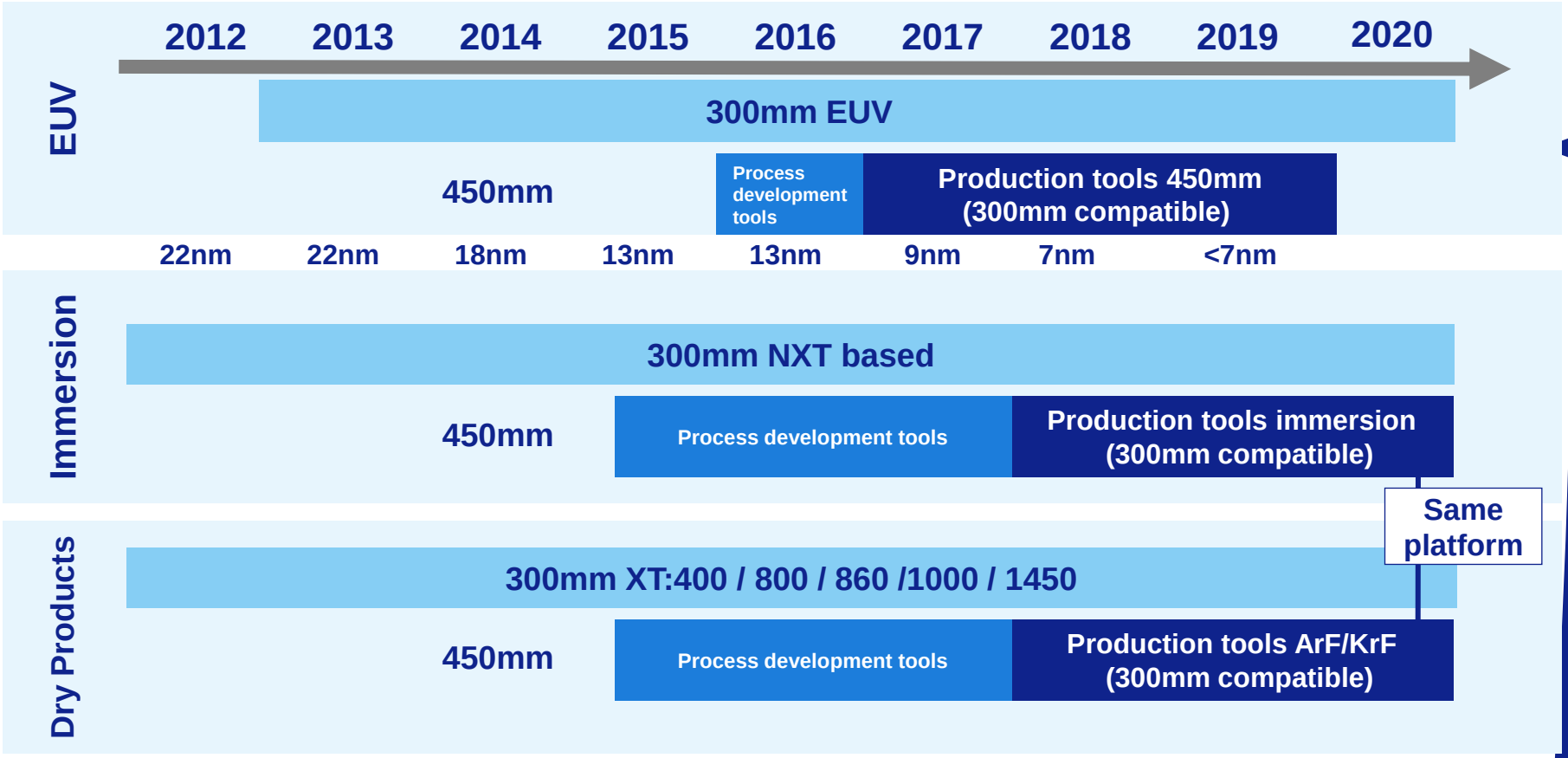
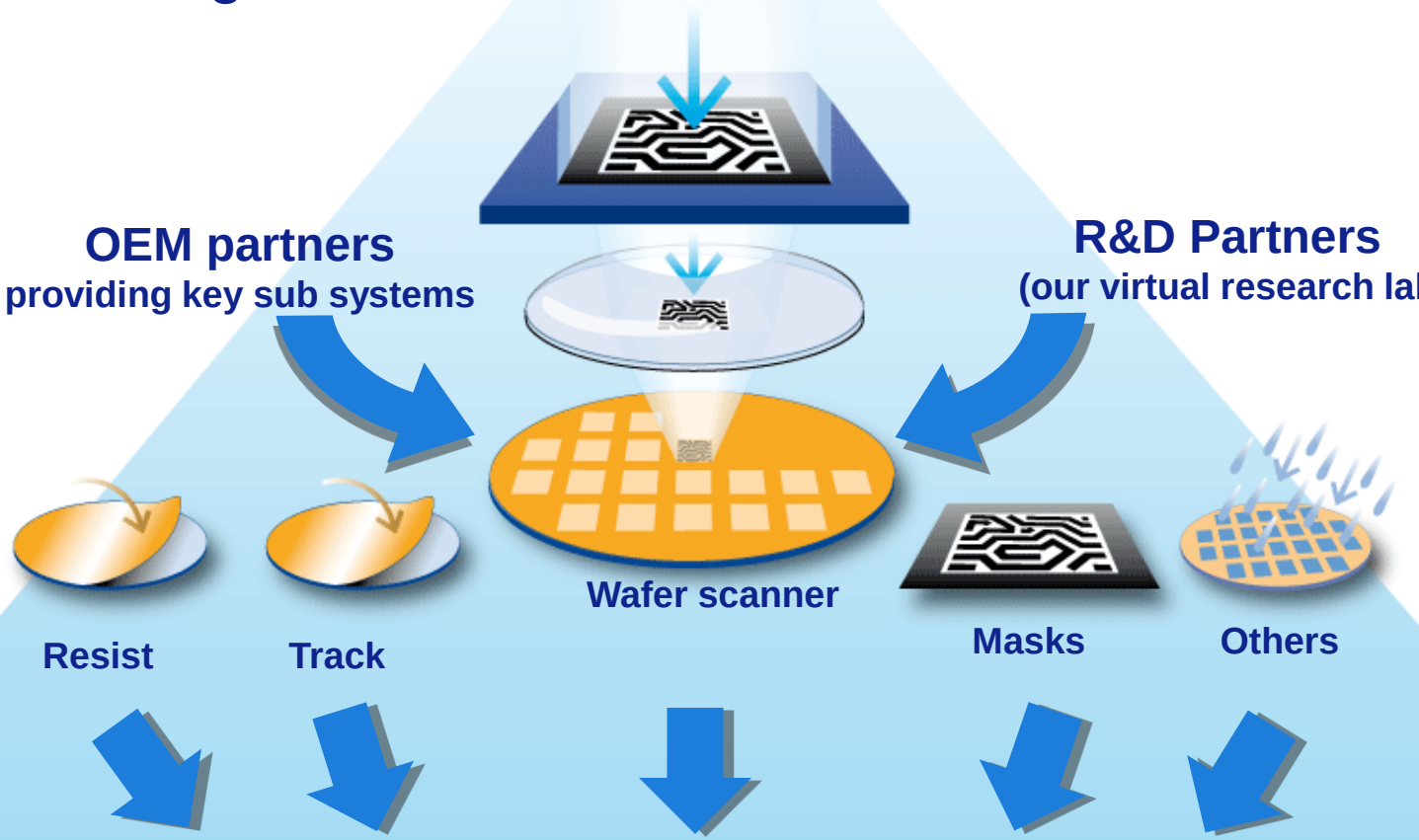
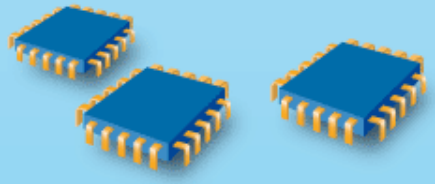
ASML enhanced development roadmap



ASML's success is the result of an integrated knowledge network



Semiconductor device manufacturers



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